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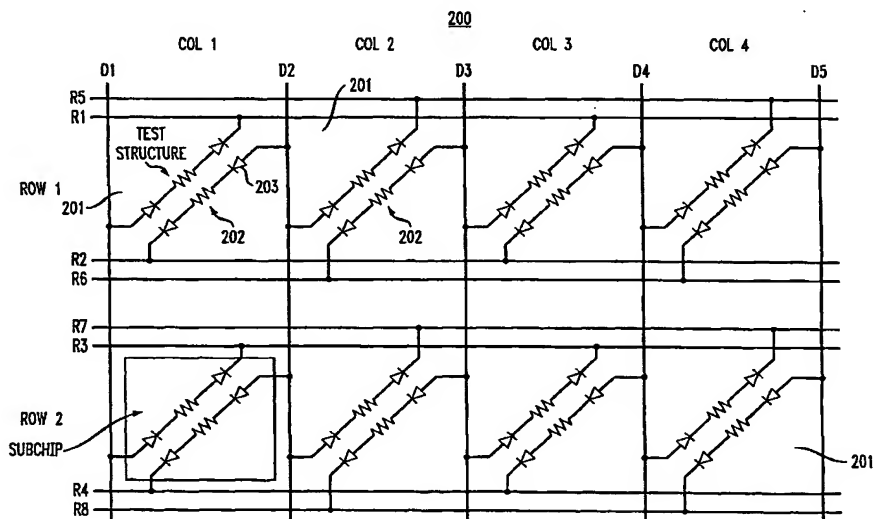
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(54) Title: METHOD AND CONFIGURATION FOR CONNECTING TEST STRUCTURES OR LINE ARRAYS FOR MONITORING INTEGRATED CIRCUIT MANUFACTURING



(57) Abstract: A test chip comprises at least one level having an array of regions. Each region is capable of including at least one test structure. At least some of the regions include respective test structures. The level has a plurality of driver lines that provide input signals to the test structures. The level has a plurality of receiver lines that receive output signals from the test structures. The level has a plurality of devices for controlling current flow. Each test structure is connected to at least one of the driver lines with a first one of the devices in between. Each test structure is connected to at least one of the receiver lines with a second one of the devices in between, so that each of the test structures can be individually addressed for testing using the driver lines and receiver lines.

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